Claims

[c1] WHAT IS CLAIMED IS:

1. A method of saving/restoring a processor state after a processor entering/exiting a debug mode, the method comprising:

storing an address of a resume instruction into the data storage space, when the processor intends to enter the debug mode;

performing a debugging instruction during the debug mode without need an actual track on the number of program counter (PC) for the debugging instruction being executed in the debug mode; and

fetching the address of the resume instruction from the data storage space, when the processor intends to exit the debug mode.

[c2] 2. The method of claim 1, wherein the data storage space is provided by an data storage device.

[c3] 3. The method of claim 1, wherein the data storage space is provided by a register.

[c4] 4. The method of claim 1, wherein the data storage space is a new instruction address.

[c5] 5. A debugging method for a debugger associating with a processor, the method comprising:

storing a program counter (PC) of a processor state with respect to a resume instruction into a data storing space in the debugger, when a debug mode is desired;

performing a debugging instruction by the debugger during the debug mode without need of an actual track on the number of PC for the debugging instruction being executed in the debug mode; and

fetching the PC of the resume instruction at the data storing space for the processor, when the debug mode is exited.

[c6] 6. The method of claim 5, wherein the data storage space is provided by an data storage device.

[c7] 7. The method of claim 5, wherein the data storage space is provided by a

register.

[c8] 8. The method of claim 5, wherein the data storage space is a new instruction address.

[c9] 9. A resume register, suitable for use in a debugging system for storing a resume address of a resume instruction in a debug mode, the resume register comprising:

a first multiplexer, receiving a program counter (PC), a debugging data, and a control signal for entering the debug mode, wherein the multiplexer also receives a force-resume signal to select the debugging data or the PC;

an OR logic gate, receiving the control signal for entering the debug mode and the force-resume signal, and exporting an output signal;

a first flip-flop, receiving the output signal of the OR logic gate and an output data from the first multiplexer, and exporting the resume address under control by the output signal of the OR logic gate;

a second multiplexer, receiving the PC and the resume address from the first flip-flop, and a control signal for exiting the debug mode; and

a second flip-flop, receiving an output data of the second multiplexer and exporting the PC,

wherein when the control signal for entering the debug mode is set by the debugging system to the first multiplexer, the first flip-flop saves the current PC as the resume address with respect to the resume instruction,

wherein when the control signal for exiting the debug mode is set by the debugging system to the second multiplexer, the second flip-flop loads the resume address and exports the resume address as the PC with respect to the resume instruction.

[c10] 10. The resume register of claim 9, wherein when the force-resume signal for the first multiplexer is set to assign a new instruction address for the resume address, the debugging data is selected for inputting the new instruction address while entering the debug mode.

[c11] 11. A resume register, suitable for use in a debugging system for storing a resume address of a resume instruction in a debug mode, the resume register

comprising:

a first flip-flop, receiving a program counter (PC) as the resume address, a control signal for entering a debug mode;

a multiplexer, receiving the PC and the resume address from the first flip-flop, and a control signal for exiting the debug mode; and

a second flip-flop, receiving an output data of the multiplexer and exporting the PC,

wherein when the control signal for entering the debug mode is set by the debugging system to the first flip-flop, the first flip-flop saves the current PC as the resume address with respect to the resume instruction, and when the control signal for exiting the debug mode is set by the debugging system to the multiplexer, the second flip-flop loads the resume address and exports the resume address as the PC with respect

to the resume instruction.